Twenty-Five Years of Single-Stage Buck–Boost Inverters

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Development and Challenges

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Single-stage buck–boost inverters have overcome the shortcomings posed by conventional voltage source inverters (VSI) and current source inverters (CSI). VSIs can produce only ac waveforms with a value less than or equal to the applied dc-link voltage (the buck mode), and CSIs can produce only ac waveforms with values greater than or equal to the applied dc-link voltage (the boost mode). On the other hand, single-stage buck–boost inverters can provide a stepped-up/down output voltage, thus accommodating a wide input voltage range. The literature claims single-stage buck–boost inverters are more efficient, less bulky, and able to operate across a wide input voltage range. So why does the industry still love conventional VSIs with a back-ended dc–dc converter or a step-up transformer?

History and State of the Art

In 1995, Caceres and Barbi proposed a double-boost differential inverter, shown in Figure 1(a) [1], that was capable of single-stage buck and boost operations. Then, in 2003, Peng introduced an impedance source inverter, presented in Figure 1(b) [2], with the same capabilities. Single-stage buck–boost inverters have now been in development for 25 years. Numerous differential and impedance source topologies have been reported for

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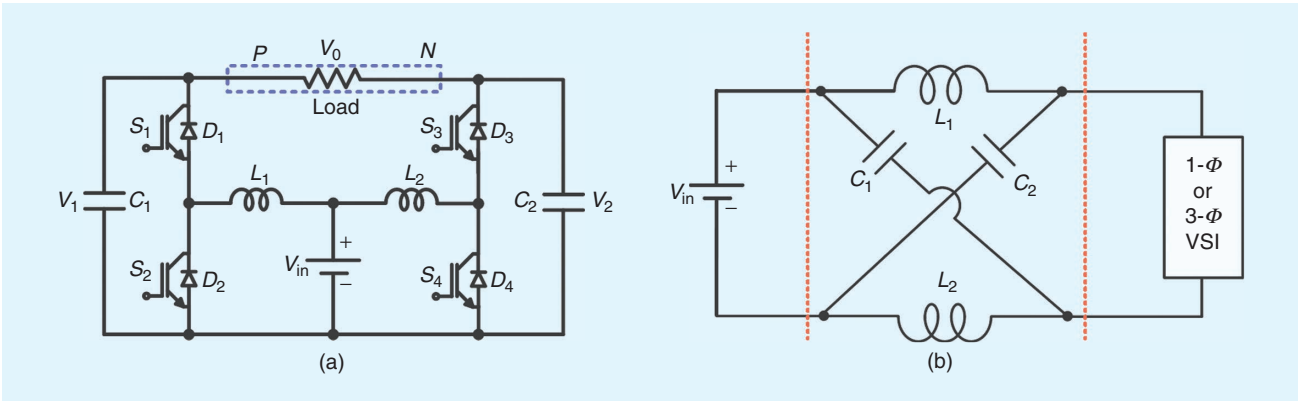

FIGURE 1 – The first reported (a) differential buck–boost inverter [1] and (b) impedance source inverter [2].

various platforms; however, to the author's best knowledge, the industry is not using them. On the other hand, many variations of VSIs, such as multilevel inverters, neutral-point clamped (NPC) inverters, and T-type inverters, have been sufficiently developed for use. This article aims to understand why single-stage topologies fail to find industrial uptake. At the same time, as per the literature, single-stage topologies have emerged as the best fit for many applications, ranging from photovoltaic (PV) integration, distributed energy resources, and electric vehicles. Has there been too little time to get these magnificent (according to the research) power converter topologies into the real world?

The most promising avenue for utilizing single-stage topologies stems from PV integration and applications. Out of all PV integration, approximately 99% is for grid-tied functions [3]. Integrating PV modules into the grid is possible only by the use of power conditioning systems (PCSs). Since PCSs act as an interface between a PV system and a grid, their task can be categorized into the following two segments:

- *PV-side requirements*: These include PV power extraction using maximum power point tracking (MPPT) and power decoupling [4].
- *Grid-side requirements*: These are specific to geographic areas and are governed by many national and international standards, such as Verband der Elektrotechnik 4105, International Electrotechnical Commission 61727 and EN 61000-3-2, and IEEE 1547, [5], [6]. The following are usually set by the standards:
  - total harmonic distortion
  - injected dc current limits
  - grid frequency range
  - common-mode leakage currents through the ground.

PCSs also need to provide ancillary services, such as active/reactive power control, voltage/frequency support, and islanding.

There have been many papers that examined single-stage topologies and emphasized single-stage grid-tied topologies [5], [7], three-phase topologies, modulation schemes [8], [9], and impedance source inverters [10], [11]. But those reviews provided an analytical and segment-specific comparison of available topologies. The present work aims to study single-stage buck–boost inverter topologies for their suitability to industry. A total of 54 topologies was analyzed for translatability into an industrial converter, with a focus on home-use PV inverter segments covering single-phase and three-phase applications. There are two main types of single-stage buck–boost inverters, i.e., differential and those based on impedance source networks (ZSNs). Developed key topologies and their respective connection types and booster circuits, by year, appear in Figure 2

Roadblocks to Industrial Uptake

It is well known that one of the main concerns for developing any industrial product is the bill of material (BOM) cost and complexity. Furthermore, a converter's net weight and net volume (including passive components and the heat sink) play an essential role in industrial uptake. Any topology leading to a higher BOM cost and complexity or to massive weights and volumes makes a product expensive and bulky and thus less attractive. Additionally, a converter's efficiency and reliability have been identified among the major design challenges for future power electronic research and development (Figure 3) [12]. Previous research shed light on the efficiency and operation of these converters, which proved to perform well [5], [10], [11]. Given that industry has failed to adopt single-stage buck–boost inverters, we hypothesized that the devices tend to have a higher BOM cost, complexity, weight, and volume. To validate the hypothesis, the cost, weight, and volume were quantitatively estimated for reported converters versus the conventional industrial solutions.

Estimating the actual converter weight, volume, and material cost from the reported topologies is extremely difficult without prototyping a device. Even if a prototype is developed, the final product, including the necessary packaging, will be significantly different than the original. We used indices as proxies for quantitative estimates of the cost, weight, and volume. The indices, along with how they function, are discussed in the following.

Stored Passive Element Energies

The maximum energy stored in the capacitive and inductive elements is a measure of a converter topology's volume and weight [13]. Additionally, this parameter tends to relate to the linear

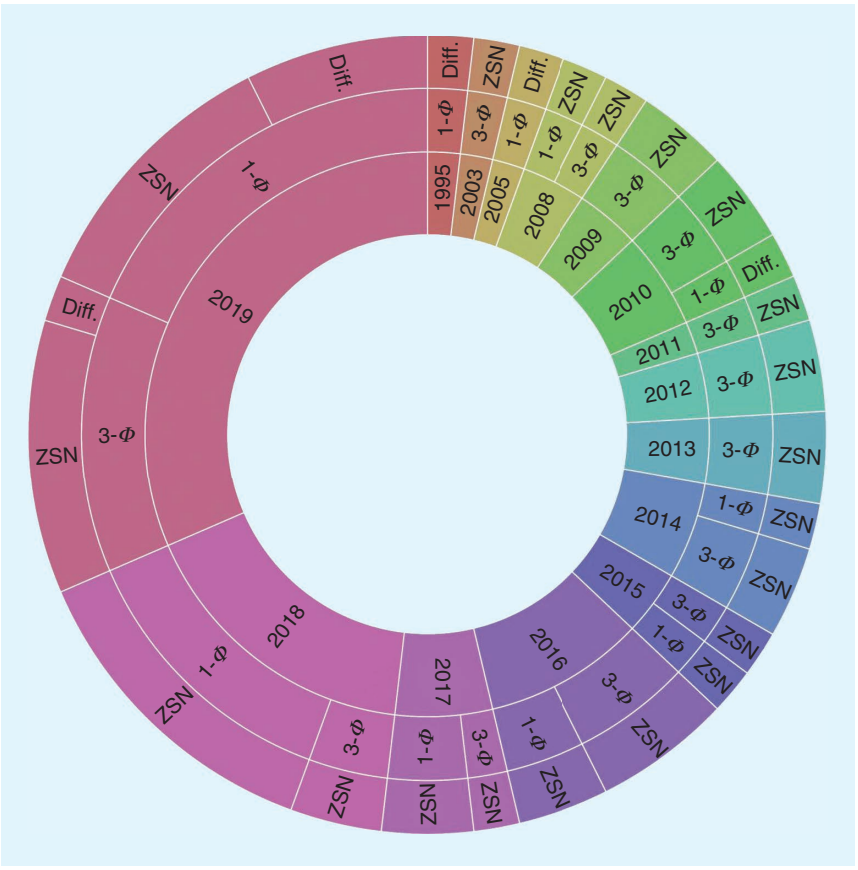

FIGURE 2 – Reported topological bifurcations by year, based on the connection type and the booster circuit, i.e., differential or impedance source network (ZSN). Diff: differential.

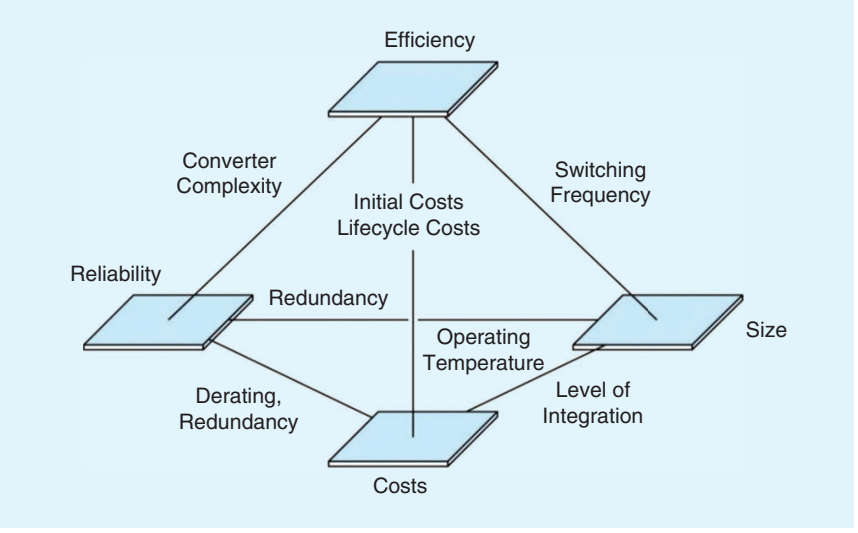

FIGURE 3 – Design challenges for future power electronics research and development[12].

cost of the passive components. The stored energy in the inductor (L_E) and in the capacitor (C_E) is given by (1) and (2), respectively:

$$L_E = \frac{1}{2}\sum LI^2, \qquad (1)$$

where L is the value of the inductor in henrys and I is the average current across the inductor in amperes;

$$C_E = \frac{1}{2}\sum CV^2, \qquad (2)$$

where C is the value of the capacitor in farads, and V is the peak voltage across the capacitor in volts.

But, as the reported topologies have varying power levels, new indices have been introduced for better comparisons based on normalized power levels. These indices include the normalized inductive storage (L_{EN}) and the normalized capacitive storage (C_{EN}), and they are obtained by dividing (1) and (2) by a topology's peak power output. The indices are obtained in (3) and (4), respectively:

$$L_{EN} = \frac{L_E}{P} = \frac{1}{2P}\sum LI^2, \qquad (3)$$

$$C_{EN} = \frac{C_E}{P} = \frac{1}{2P}\sum CV^2, \qquad (4)$$

where P is the peak output power in watts.

Switching Component Count

Here, we focus on the total number of diodes (N_D) and the total number of switches used in a topology (N_S). As the number of semiconductor components increases, the circuit operation's losses and complexity grow considerably. But some new topologies, such as NPC converters and T-type inverters, use a higher number of switches to relieve device stress. Therefore, N_S and N_D are not conclusive performance indices when viewed independently; when considered with their respective device ratings, they form a reasonable basis of comparative assessment.

Switching Device Rating

The *total device rating* (*TDR*) is defined as the sum of the switching devices' individual ratings, which are the product of their peak voltage and their peak current. The TDR is a quantifiable measure of switching device stress as well as associated cost factors [14]. But because all the reported topologies have different power ratings, the normalized TDR for the diodes and switches is defined as the TDR divided by a converter's power rating. These indices are given by (5) and (6), respectively, where D_{RN} is the normalized diode rating and S_{RN} is the normalized switch rating:

$$D_{RN} = \frac{1}{P}\sum VI, \qquad (5)$$

$$S_{RN} = \frac{1}{P}\sum VI, \qquad (6)$$

where V and I are the peak voltage and the peak current across the respective switching component and P is the peak power rating of the topology in watts.

The preceding ratings of the investigated topologies are numerically calculated and compared against benchmarks based on reference designs available from application notes prepared by leading industries [15]–[17]. A total of 27 single-phase and 27 three-phase topologies reported for various platforms were investigated and compared with benchmark converters 1 phase benchmark (P-BM) and 3 P-BM, respectively. The comparative evaluation is given in Table 1 for the single-phase topologies and in Table 2 for the three-phase topologies. In the tables, the cells are green when the performance indices of an investigated topology are better than the benchmark, and they are blue when a topology's values are worse than the benchmark. Red cells indicate the benchmark performance indices, while brown ones show general attributes.

TABLE 1 – SINGLE-PHASE BUCK–BOOST INVERTERS.

REFERENCE	CONNECTION	BOOSTER CIRCUIT	POWER (KW)	L_{EN} (J/KW)	C_{EN} (J/KW)	N_D	D_{RN}	N_S	S_{RN}
1 P-BM*	1-Φ	PFCB plus inverter	750	0.02	63.54	2	5.07	2	5.07
[1]	1-Φ	Differential	500	0.5	8.45	0	NA	4	65
[18]	1-Φ	Differential	1,500	0.38	2.7	0	NA	4	60
[19]	1-Φ	Differential	250	0.05	1.7	0	NA	4	39.81
[20]	1-Φ	Differential	250	0.21	29.4	0	NA	8	116
[21]	1-Φ	Differential	300	0.01	92.04	8	90.73	4	78.33
[22]	1-Φ	Differential	500	0.18	0.72	2	21.52	4	43.04
[23]	1-Φ	Differential	800	0.22	0.27	0	NA	6	37.5
[24]	1-Φ	ZSN	500	1.53	6.27	2	92.4	4	184.8
[25]	1-Φ	ZSN	500	0.1	0.48	0	NA	8	20.4
[14]	1-Φ	ZSN	250	3.76	58.75	6	120	5	100
[26]	1-Φ	ZSN	100	0.42	1.23	2	65.6	5	60.8
[27]	1-Φ	ZSN	300	0.49	75.28	2	14.47	5	36.17
[28]	1-Φ	ZSN	1,100	0.06	0.2	8	22.04	8	22.04
[29]	1-Φ	ZSN	300	0.13	0.36	0	NA	4	62
[30]	1-Φ	ZSN	300	0.22	1.11	4	45	4	45
[31]	1-Φ	ZSN	800	0.08	108.82	6	14.8	4	9.87
[32]	1-Φ	ZSN	250	0.3	51.98	2	76	5	190
[33]	1-Φ	ZSN	500	0.15	42.5	3	11.25	5	18.75
[34]	1-Φ	ZSN	200	0.15	44	0	NA	5	75
[35]	1-Φ	ZSN	500	0.23	2	7	28	6	24
[36]	1-Φ	ZSN	500	0.12	49.16	7	50.4	5	27
[37]	1-Φ	ZSN	200	4.3	62.17	2	27.5	4	30
[38]	1-Φ	ZSN	200	2	7.41	2	31	5	77.5
[39]	1-Φ	ZSN	250	0.67	219.2	5	33	5	16.5
[40]	1-Φ	ZSN	500	0.18	0.54	4	49.6	6	52.7
[41]	1-Φ	ZSN	500	0.4	120.84	6	24.96	2	30
[42]	1-Φ	ZSN	200	0.03	7.34	1	12.5	5	75

*1 P-BM is the benchmark for a single-phase industrial transformerless inverter reference design [15].

PFCB: power factor correction boost converter.

Single-Phase Topologies

As shown in Table 1, no topology has performance indices that are all better than the benchmark. The following factors are considered:

- All reported topologies use a higher S_{RN} and D_{RN}, which is a significant cost factor (it increases the BOM expense, which is a major letdown for industry).
- All topologies except [21] have a higher L_{EN}, which dictates their weight.
- The C_{EN} values of most of the reported single-stage buck–boost topologies seem to be better than the benchmark. However, with a closer look, this result is due to the absence of double-line frequency input power oscillation decoupling. For a practical PV application to implement MPPT, the double-line frequency input power oscillation has to be removed through a revised design to achieve a constant input current. The benchmark mitigates this problem by providing optimal power decoupling through an increased C_{EN}.

Three-Phase Topologies

Similar to the single-phase case, none of the reported three-phase topologies has performance indices that are all better than the benchmark, as detailed in Table 2. The following issues are relevant.

- All the topologies have a higher L_{EN}, which dictates their weight.
- Most of the topologies (20 out of 27) use a larger capacitive energy storage (C_{EN}).
- All reported topologies except [49] and [62] use a higher D_{RN}.
- It seems that most of the topologies use fewer devices than the benchmark. Due to the lack of available industrial reference designs that have a power level similar to that of the reported converters (~1–3 kW), we used a reference design with a higher power (10 kW). To efficiently cater to the greater power, the benchmark design uses an NPC three-level inverter and an

TABLE 2 – THREE-PHASE BUCK–BOOST INVERTERS.

REFERENCE	CONNECTION	BOOSTER CIRCUIT	POWER (KW)	L_{EN} (J/KW)	C_{EN} (J/KW)	N_D	D_{RN}	N_S	S_{RN}
3 P-BM*	3-Φ	Booster plus three L3PI	10,000	0.01	17.28	2	4.80	14	24
[43]	3-Φ	Differential	1,250	3.24	0.12	6	28.8	6	28.8
[44]	3-Φ	Differential	3,000	0.07	9	0	NA	6	32
[2]	3-Φ	ZSN	3,500	0.04	32.06	0	NA	6	17.23
[45]	3-Φ	ZSN	1,000	0.04	3.13	1	7.5	6	45
[46]	3-Φ	ZSN	250	0.2	17.25	2	8.4	7	42
[47]	3-Φ	ZSN	250	0.72	0.3	2	8	7	28
[48]	3-Φ	ZSN	2,000	6.4	36	7	105	6	90
[49]	3-Φ	ZSN	250	0.5	148.72	1	4.2	6	25.2
[50]	3-Φ	ZSN	500	2.03	105.8	4	47.84	6	248.16
[51]	3-Φ	ZSN	500	1.32	21.6	1	10	6	60
[52]	3-Φ	ZSN	800	0.87	17.58	3	140.63	6	281.25
[53]	3-Φ	ZSN	500	1.8	176	13	156	6	72
[54]	3-Φ	ZSN	250	0.8	160	1	8	6	48
[55]	3-Φ	ZSN	800	0.06	19.01	3	21.94	6	33.75
[56]	3-Φ	ZSN	350	1.14	87.5	5	150	7	107.14
[57]	3-Φ	ZSN	620	0.11	66.93	5	24.19	6	29.032
[58]	3-Φ	ZSN	2,000	0.16	5.04	3	12.3	6	24.6
[59]	3-Φ	ZSN	1,500	0.6	5.27	3	86.1	6	36.08
[60]	3-Φ	ZSN	500	0.65	222.31	5	33.1	6	23.58
[61]	3-Φ	ZSN	900	0.99	12.27	6	68.27	7	49.53
[62]	3-Φ	ZSN	1,000	0.27	18.8	1	4	6	24
[63]	3-Φ	ZSN	800	0.5	39.13	5	28.16	6	58.08
[64]	3-Φ	ZSN	500	0.32	79.2	0	NA	9	42
[65]	3-Φ	ZSN	500	1.94	20.25	4	88	6	108
[66]	3-Φ	ZSN	1,000	0.1	145.8	9	36.45	12	32.4
[67]	3-Φ	ZSN	500	NA	39.6	2	12	8	30
[68]	3-Φ	ZSN	400	0.72	110.16	5	53.13	7	119

*3 P-BM is a benchmark formed from a combination of a boost converter [16] and a three-phase three-level inverter [17] reference design.

L3PI: level 3-phase inverter.

interleaved boost converter with two parallel branches, leading to a higher device count. A simple boost converter back end with a two-level three-phase inverter (a suitable solution for the ~1–3-kW power range) requires only seven switches and one diode. Compared to this modified benchmark metric (N_D: 1; N_S: 7) none of the reported topologies offers a significant advantage in terms of the number of devices.

- Even though the number of devices in the reported topologies is lower than the benchmark, the normalized switch rating of all the topologies except [2] is higher than the benchmark.

Conclusion

For 25 years, extensive research has been reported for single-stage buck–boost converters for single- and three-phase applications. Both differential and ZSN-based converters are equally popular in the literature. Single-stage buck–boost inverters have several functional advantages over the conventional designs popular in the industry (inverters with back-end dc–dc converters), such as a wide input voltage range capability, a higher efficiency, a lower weight, and a smaller volume. Despite such functional advantages, they fail to gain industrial uptake. A thorough review of the literature about these converters, covering more than 50 topologies, was presented in this article to investigate the situation.

Converter cost and size constitute two of the main design challenges for future power electronics development and heavily influence industrial popularity. Performance indices, such as the normalized energy content of the passive elements, number of power electronic devices, and normalized device rating, were used as proxy estimates for the size (weight and volume) and cost of the reported topologies. A quantitative comparison of these performance indices revealed that single-stage buck–boost inverters tend to have higher costs and larger sizes. These disadvantages apply across the number of phases (single-phase and three-phase) and the converter topology (differential and ZSN). Future research to reduce the normalized passive energy content [$(1/2P)LI^2$ for the inductor and $(1/2P)CV^2$ for the capacitors] and the normalized device rating [$(1/P)\Sigma VI$] for the diodes and switches] will make these topologies more suitable for practical application.

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